Low Power Passive Equalizer Design for Computer Memory Links

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Abstract

Several types of low power passive equalizer is proposed and optimized in this work. The equalizer topologies include T-junction, parallel R-C and series R-L structures. These structures can be inserted at driver or/and receiver side at either the chip or package level and the communication bandwidth can be improved with little overhead on power consumption. Using the area of the eye as the objective function to be maximized, we optimized these equalizers for the CPU-memory interconnection of an IBM POWER6^{TM} System with and without practical constraints on the RLCG parameter values. Our experimental results show that without employing any equalizers, the data-eye is closed for a bit-rate of 6.4 Gbps. We tried twelve different equalizer schemes and found they produce very different eye diagrams. The scheme yielding the maximum eye improves the height of the eye to more than 300 mV at a total power cost of 7.2 mW, while the scheme yielding the minimum jitter limits the jitter magnitude to 10 ps at a total power cost of 9.5 mW. We also have shown that the solution resulting from the proposed optimization approach have very small sensitivity to the tolerance of the R,L,C values and the magnitude of the coupled noise.

1. Introduction

The power and performance of packaging level interconnects have become crucial for the whole system performance. While the multi-core architecture increases the on-chip computing capability, inter-chip communication bandwidth has to be expanded to accommodate the demand. Meanwhile, how to control the signaling power is becoming an ever greater challenge since many approaches that improve performance make the system more power hungry, therefore a low power signaling scheme is needed.

As an important approach to reduce the inter-symbol interference(ISI), various equalization schemes have been widely used. In 1920's, the concept of equalization was introduced in [1],[3]. In [8], a constant-R ladder network (Fig. 1) was described, which can also be used as an equalizer. The ladder satisfies the condition $z_1 z_2 = R^2$. When it is terminated with resistance R, its input impedance is R as well, therefore multiple ladders can be cascaded.

In 2005, [11] proposed an adaptive passive equalizer based on a RLC T-junction network with tunable resistance parameter. It claims better power efficiency than active equalizer. Shin et al. from Intel proposed three passive equalizers in [10] that are used at the driver side. The equalization schemes include T-junction and parallel R-C, and have demonstrated that 90mV eye opening at 10GHz is feasible for a 19-inch long differential pair with 1.2V supply voltage on actual measured hardware.

In this paper, we propose a set of very simple and effective passive equalizer schemes for CPU-memory links that can be used at both driver and receiver sides and with very low power consumption. Within the practical size limits, the equalizer schemes greatly improve the eye quality even when crosstalk is being considered. The basic components include T-junction, parallel R-C and series R-L structures. Combining these components in different ways we can have various equalization schemes, as shown in Table 1. Due to the low pass characteristic of typical transmission lines, high frequency components in the input signals have a much larger attenuation than low frequency components, which causes ISI and limits the communication bandwidth. The T-junction, parallel R-C and the series R-L structures act as a high-pass filter and therefore compensate the magnitude of different frequencies. By doing so, we can alleviate the ISI and improve the interconnect performance.

Our contribution in this work includes the following: 1) we propose a set of passive equalizer schemes, 2) we employ the schemes on the CPU-memory link of IBM POWER6^{TM} system, and observe significant performance improvement with little power overhead, 3) we compare and analyze the different results of these schemes, 4) we demonstrated that our approach is not sensitive to the variations of the RLC components, and robust to crosstalk effect.

2. The CPU-memory links in IBM POWER6^{TM} system

We simulate the passive equalizer schemes on the CPU-memory link of IBM POWER6^{TM} system. IBM introduced POWER6^{TM} microprocessor-based systems in 2007. The dual-core microprocessor has been fabricated in a 65 nm SOI process and contains over 700 M transistors. It can operate at over 5GHz frequency for high-performance applications and consumes less than 100 W for low power applications [5]. Due to these two modes of operation both the speed and the power are important design considerations for the POWER6^{TM} I/O circuitry and a challenge for the corresponding interconnection design.

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Table 1. Equalizer schemes

Index	Driver side	Receiver side
Group 1: matched driver + matched receiver		
A	Z_0	Z_0
B	On-chip T-junction	On-chip T-junction
Group 2: unmatched driver + matched receiver		
C	On-chip R-C	Z_0
D	On-chip R-C	On-chip T-junction
Group 3: matched driver + unmatched receiver		
E	Z_0	On-chip R-C
F	Z_0	On-chip R-L
G	On-chip T-junction	On-chip R-C
H	On-chip T-junction	On-chip R-L
Group 4: unmatched driver + unmatched receiver		
I	On-package T-junction	On-package T-junction
J	On-package T-junction	On-chip R-C
K	On-package T-junction	On-chip R-L
L	On-chip R-C	On-chip R-C
M	On-chip R-C	On-chip R-L

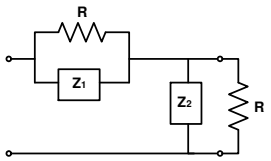

Figure 1. Constant-R ladder: input impedance is R when $z_1 z_2 = R^2$

According to [4], there are more than 800 wires coming off the processor chip dictated by system performance and scaling requirements. The total I/O bandwidth is around 300 GBps. The links between CPU and memory have bit-rate up to 3.2Gbps/wire for single ended and 6.4Gbps/wire for differential pair.

Each POWER6^{TM} chip includes two integrated memory controllers [6]. A memory controller supports up to four parallel channels, each of which can be connected through an off-chip interface to one to four buffer chips daisy-chained together. A channel supports a 2-byte read datapath, a 1-byte write datapath, and a command path that operates four times faster than the DRAM frequency, which is up to 800-MHz. For some system configurations, buffer chips are mounted on the system board, through industry-standard DIMMs (dual inline memory modules) card. We use the off-chip CPU-memory links as our test case of the proposed equalizer schemes because the approach can improve the signal quality with little overhead on power consumption.

The channel is a 20 inches long differential pair, and we perform the test at an operating frequency of 6.4 GHz. The representative critical path of the channel, from the chip carrier through card, board, to memory module is modeled and analyzed. The model takes all the fan-out, connector, and via array discontinuities into account. We observe waveforms at the input to the CPU module, at output from memory module, and three internal ports as shown in Fig. 2. Port a is at the interface of the CPU, Port b is between the board trace and DIMM connector and Port c is from DIMM trace to memory module.

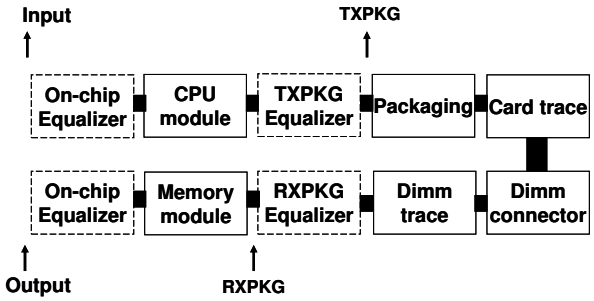

Figure 2. Structure of the CPU-memory link

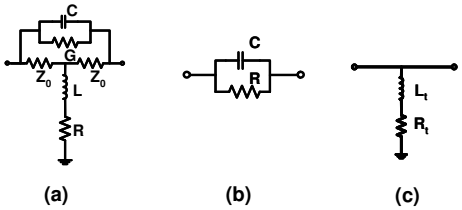

Figure 3. equalization components: (a) T-junction (b) R-C (c) R-L

3. Equalization Structures and Schemes

We use three basic equalizer components: T-junction, R-C and R-L, as shown in Fig. 3. To preserve the constant R property, the RLCG components in T-junction satisfy:

$$RG = Z_0^2, \frac{L}{C} = Z_0^2 \tag{1}$$

The T-junction and R-C may be used at both sides of the channel, while we only use R-L at receiver side. Both on-chip and off-chip implementations can be employed for all the three structures, as shown in Table 1 and Fig. 2. For on-chip implementation, the equalizers are put before CPU module and after memory module. For on-package implementation, the equalizers are put after CPU module and before memory module. The positions of ports input, TXPKG, RXPKG and output are also shown in Fig. 2. We divide the twelve schemes in Table 1 into four groups according to the matching conditions at both sides, because the matching conditions have great impact on the eye-diagram. With matched driver or receiver, there will be no or only one reflection when the signal is propagating and therefore the jitter is small. With unmatched driver or receiver, there will exist reflections affecting the height of the eye.

In Table 1, group 1 includes the original channel without using equalizer (scheme A), and using on-chip T-junction at both sides

Table 2. Difference between on-chip and off-chip equalization

Structure	R_s at driver side	R_{load} at receiver side
R-L	NA	Inf
R-C	10Ω	Z_0
On-chip T-junction	Z_0	Z_0
Off-chip T-junction	10Ω	Z_0

Table 3. Optimization results without size limit

Idx	Optimal solution						Performance			
	$R_d(\Omega)$	$C_d(pF)$	$R_t(\Omega)$	$L_t(nH)$ or $C_t(pF)$	$R_{DC}(\Omega)$	$R_{AC}(\Omega)$	$V_{eye}(V)$	$Jitter(ps)$	$Power(mW)$	f
A	NA	NA	NA	NA	100	100	NA	NA	7.54	NA
B	11.78	72.00	61.56	10.58	100	93	0.168	15.4	8.73	11.83
C	2.54	92.58	NA	NA	63	111	0.244	20.1	10.14	16.61
D	43.56	2.72	97.08	31.95	104	118	0.240	20.0	7.36	16.36
E	NA	NA	73.97	5.14	174	159	0.153	29.6	3.35	9.69
F	NA	NA	26.24	3.97	76	164	0.230	27.7	9.92	14.79
G	33.24	6.22	18.47	40.00	106	164	0.170	20.0	9.24	11.58
H	32.64	12.00	51.12	3.67	100	71	0.220	14.2	9.70	15.63
I	12.31	57.21	55.63	8.60	60	53	0.244	43.0	12.92	13.82
J	76.64	2.00	20.71	40.00	63	58	0.244	12.8	15.81	17.50
K	56.41	3.92	43.69	2.00	59	52	0.310	25.6	16.18	20.25
L	38.70	3.67	32.85	18.04	130	116	0.234	29.4	5.29	14.84
M	53.56	4.53	46.14	2.39	110	124	0.307	26.8	7.18	19.87

R_{DC} is the total DC resistance, R_{AC} is the total AC resistance, V_{eye} is the eye opening and f is the cost function.

(scheme B). $R_s = Z_0$ is added between the source and the T-junction, and $R_{load} = Z_0$ is added between the T-junction and ground. For on-chip implementation, we do not adopt Ladder structure because for this link T-junction can achieve the same eye quality as Ladder that consumes less power. We do not list matched T-junction structure for on-package implementation since experiments show they have very similar eye diagram. By substituting the equalizer used in Group 1 at the driver's side with on-chip R-C, we have the two schemes C and D in group 2. The unmatched driver side equalization becomes more effective when the source is ideal ($R_s = 0$). To take the non-ideal factor into account, we assume $R_s = 10\Omega$. In group 3, the unmatched receiver equalizer can be either R-C or R-L. When R-C structure is used, we add $R_{load} = Z_0$ between the output port and ground to avoid open termination. As shown in group 4, we use on-package T-junction only under unmatched condition with $R_s = 10\Omega$ and we expect to see larger eye due to the reflections. The usage of different structures are summarized in Table 2.

4. Simulated Annealing Optimization flow

With the values of R, L, C, G components as variables, we can improve the equalizer by using optimization algorithms. There are at most two equalizers for a given problem, and each equalizer can be determined by two parameters, if we use Eq.1. We label the parameters with subscript d for driver side and t for receiver side. In this way, we can present the solution for the schemes with R-C structure at receiver side as $s = (R_d, C_d, R_t, C_t)$, and for other schemes as $s = (R_d, C_d, R_t, L_t)$. Since we want to maximize eye-opening and minimize jitter, we define a cost function as

$$f(s) = \frac{1}{2} V_{eye} \times (T_c - jitter) \tag{2}$$

in which $f(s)$ indicates the area of the eye, T_c is the cycle time, and eye-opening V_{eye} and $jitter$ are derived by method in [9], which provides a fast evaluation tool for the optimization task. When the eye is closed, [9] gives jitter that equals to cycle time and eye opening less than zero. This metric has been widely used to evaluate the eye quality [2]. Given the fact that $f(s)$ is a highly non-linear function, and the four variables form solution space with dimension of four, we use Simulated Annealing algorithm [7] to find the optimal solution. The acceptance rate function is defined as

$$P(e, e', T) = e^{\frac{e-e'}{T}} \tag{3}$$

Table 4. Sensitivity comparison

Idx	V_{eye}^{max}	V_{eye}^{min}	V_{eye} var.	J^{max}	J^{min}	$\frac{J^{min}}{T_c} - \frac{J^{max}}{T_c}$
B	0.143	0.126	12%	26.0	19.5	12.5%-16.6%
C	0.232	0.192	17%	39.6	28.4	18.2%-25.3%
E	0.154	0.123	20%	42.9	29.7	19.0%-27.5%
M	0.320	0.252	21%	39.1	26.8	17.2%-25.0%

The function $temp(k)$ is the cooling schedule which is expressed as

$$temp(k) = T_0 D^k \tag{4}$$

T_0 is the initial temperature, and $D(0 < D < 1)$ is the temperature decreasing rate.

5. Experimental Results of Optimization

We model the 20 inches long differential CPU-memory links with s-parameters and perform HSPICE simulation. The supply voltage is 1.1V and the bit-rate is 6.4 Gbps with slew rate of 45ps. We implemented the Simulated Annealing flow in Matlab and performed equalizer optimization. We compare the matched I/O results, in which all external and internal ports are matched with 100Ω differential impedance, with different equalization schemes listed in Table 1 in terms of eye quality and power consumption. Table 3 and Table 5 are the optimization results with/without consideration of size limit. When size limit is considered, the inductor should be no more than 5nH and the capacitor should be no more than 15pF. Please note that the size limit of L $\leq$ 5nH translates into C $\leq$ 2pF for T-junction at driver side. For example in Table 5, C_d in schemes G-K has reached the boundary value. The sensitivity of the optimal solution with $\pm 15\%$ variations in Table 5 is studied in Table 4. For schemes A (original), B (T-junction + T-junction), G (T-junction+RC) and M (RC+T-junction), we demonstrate their eye diagrams (Fig. 4- 7) with 640 bit long pseudo-random bit sequence as inputs. The input bit sequence is generated by 8-bit linear feedback shift register. The transfer function and input impedance for these four schemes are shown in Fig. 8. To study the crosstalk effect for the three representative schemes, We consider eight switching neighbors (four on right and four on left) with input pattern of "0101..." simultaneously. The eye diagrams with crosstalk effect as shown in Fig. 9. For completeness, the eye diagram at output of using 3-tap FFE(Feed Forward Equalization) at driver side is shown in Fig. 10. The eye opening is 0.222V and jitter is around 50ps.

Table 5. Optimization results with size limit: L $\leq$ 5nH, C $\leq$ 15pF

Idx	Optimal solution						Performance			
	$R_d(\Omega)$	$C_d(pF)$	$R_t(\Omega)$	$L_t(nH)$ or $C_t(pF)$	$R_{DC}(\Omega)$	$R_{AC}(\Omega)$	$V_{eye}(V)$	$Jitter(ps)$	$Power(mW)$	f
A	NA	NA	NA	NA	100	100	NA	NA	7.54	NA
B	0.00	2.00	21.50	5.00	100	104	0.140	24.5	7.53	9.22
C	92.6	2.54	NA	NA	153	156	0.219	28.4	5.54	14.00
D	49.70	0.00	21.56	5.00	110	160	0.132	25.2	7.06	8.65
E	NA	NA	74.00	5.14	174	159	0.152	30.7	3.35	9.54
F	NA	NA	26.00	4.00	76	164	0.230	27.7	9.98	14.79
G	64.03	2.00	37.57	15.00	106	164	0.147	11.1	9.84	10.67
H	99.56	2.00	65.11	3.75	101	59	0.196	26.3	10.48	12.74
I	29.64	2.00	24.65	5.00	60	58	0.200	26.0	14.70	13.03
J	66.05	2.00	33.23	15.00	65	56	0.241	13.2	15.13	17.24
K	100	2.00	46.81	2.19	60	52	0.303	23.9	16.85	20.05
L	33.70	4.00	36.54	15.00	130	115	0.233	31.9	5.19	14.49
M	53.56	4.53	46.14	2.39	110	124	0.307	26.8	7.18	19.87

R_{DC} is the total DC resistance, R_{AC} is the total AC resistance, V_{eye} is the eye opening and f is the cost function.

5.1 Eye-opening comparison of different schemes

First we can notice from Table 3 that unmatched driver produces larger eye opening due to reflection. In Group 1, the eye opening of scheme B is 0.168 V, and in Group 3, the eye opening is no more than 0.230 V (scheme F). With unmatched driver, the largest eye openings in Group 2 and 4 are 0.244 V and 0.310 V respectively. It is also observed that using R-L at receiver side can improve the eye-opening. For example, the eye-opening of scheme E is 0.153 V, which is increased to 0.230 V in scheme F, and scheme H enlarges the eye of scheme G from 0.170 V to 0.220 V. Similarly, the eye of scheme J and scheme L are increased to 0.310 V and 0.307 V in scheme K and scheme M, respectively.

5.2 Total power comparison of different schemes

We use pseudo-random bit sequence as input to measure the total power, which includes both AC and DC power. The total power consumption for the twelve schemes are listed in column 10 in Table 3, and in column 6 and 7, we give the total DC resistance and AC resistance to show their impact on the total power consumption. The AC resistance is measured with the input as a 3.2 GHz sin wave, which approximates the "0101..." bit-sequence. First, we can see that the DC resistance is a determinant factor. The larger the R_{DC}, the smaller the total power would be. For instance, sch.E has the largest DC resistance of 174Ω and the lowest total power of 3.35 mW, while scheme K has the smallest DC resistance of 59Ω and the highest total power of 16.18 mW. If two schemes have the same DC resistance, then R_{AC} becomes critical. For instance, scheme B and A have the same R_{DC} of 100Ω, but with smaller R_{AC}, scheme B consumes 8.73 mW, which is around 1.2 mW more than scheme A. Similarly, scheme C and J both have R_{DC} equal 63Ω, but scheme J consumes 15.82 mW, which is 5.7 mW more than scheme C because scheme J has much smaller R_{AC}.

5.3 Changes of performance when size limit is considered

When size limit constraints are added, we notice that RC variables tend to maintain their product as constant, while RL variables tend to maintain their ratio as constant. For the optimal solutions, three different trends can be observed:

1. The optimal solution changes and eye becomes worse. Scheme B, C, D, G, H, and I fall in this category.

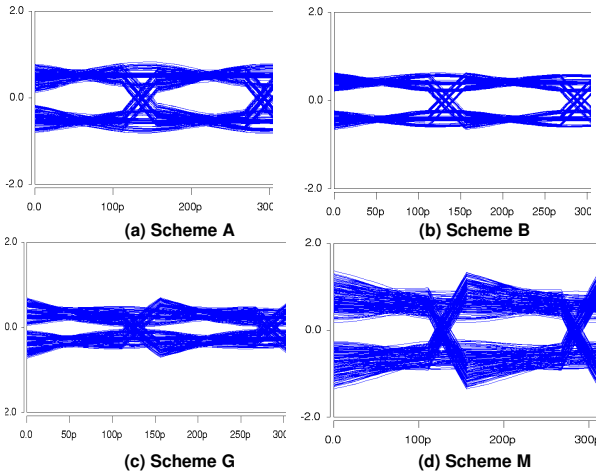

Figure 4. Eye diagram at input port

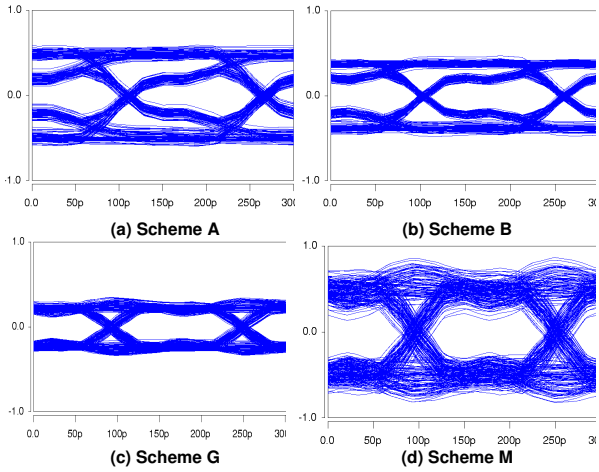

Figure 5. Eye diagram at port TXPKG

- For scheme B, the T-junction at driver side tends to reduce to Z_0 regardless of the size limit constraint, therefore the equalizing effect of T-junction at receiver side is critical. Once the size is limited, L_t is reduced from 10.58 nH to 5 nH and the eye opening becomes worse.
- For scheme C, R_d becomes very large when C_d has to reduce and therefore limits the eye opening.
- For scheme D, even when no size constraint is enforced, the high pass filter effect of the R-C structure is small because C_d is only 2.72 pF, but the T-junction has strong effect on the eye diagram with L_t as large as 32 nH. Once the size is limited, L_t reduces to 5 nH and eye diagram becomes worse.
- For scheme G as well, the equalizer at the driver side has only a small effect while the R-C structure at the receiver side plays the major role. Therefore, limiting the size hurts the performance.
- For scheme H, the driver side T-junction has greater effect than the R-L at receiver side. As a result, when C_d is forced to be 2 pF (L_d to be 5 nH), eye opening becomes worse.
- Scheme I is similar to scheme H since the T-junction placed at the driver side has a major impact on the effectiveness of the equalization. For such schedules the reduction of the C_d from 57.21 pF to 2 pF results in shorter eye opening and larger jitter.

2. The optimal solution changes but the eye remains the same. Schemes J, L and K belong to this category. The solution optimality is maintained because the RC L/R time constants have been maintained. For example, in Scheme K, the R_dC_d constant before and after considering size limit are 221 ps and 200 ps, and the L_t/R_t constants are 45.8 ps and 46.8 ps, respectively.

3. The optimal solution does not change. The optimal solutions for schemes E, F and M are already within the physical bounds before considering the size limit, therefore they have the same optimization results when size limit is enforced.

5.4 Sensitivity comparison of different schemes

To study the sensitivity of eye quality, we choose one representative schemes from each of the four groups and vary the RLGC values by $\pm 15\%$. We summarize the sensitivity comparison results in Table 4. The variation is calculated by dividing the minimum value with the maximum value. The fluctuation on eye opening is less than 21%, and the variation of jitter over cycle time is no more than 8.5%.

5.5 Eye diagram illustration of different schemes

We show the eye diagrams (Figs. 4-7) corresponding to the optimization results in Table 5. The results for schemes A, B, G and M at each port are illustrated. Our experimental results show that scheme G has the smallest jitter and scheme M has the largest eye (The row 8 and row 14 of Table 5). We can see clearly from Fig. 4 that the eye diagram of scheme M is much thicker than the others due to reflections. In Fig. 5, the DC voltage levels of scheme B and G are smaller than scheme A because the transfer function of T-junction is less than one. The eye opening of scheme A at port RXTPG becomes closed in Fig. 6. The eyes of scheme B and G are improved significantly after equalization at output port, as shown in Fig 7.

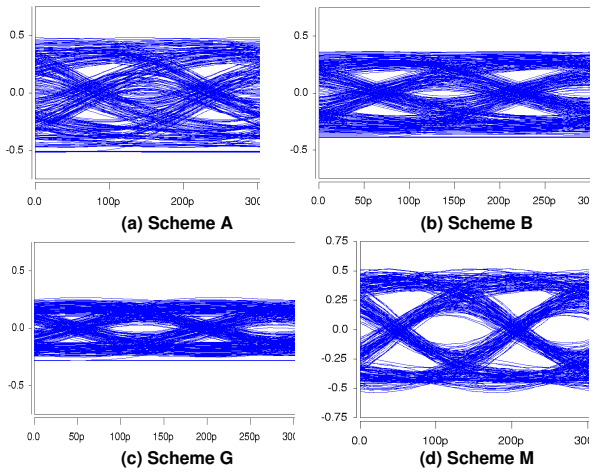

Figure 6. Eye diagram at port RXPKG

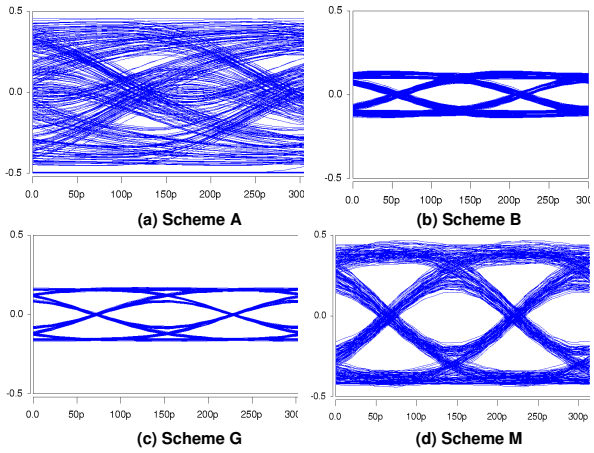

Figure 7. Eye diagram at output

5.6 Transfer function and input impedance of different schemes

The transfer function and input impedance of channels with different equalizations are given in Fig. 8. $H(s)$ of scheme B and G has small magnitude, which results lower DC voltage, but they have very high cut-off frequency that reduces jitter significantly. $H(s)$ of scheme M has larger magnitude and lower cut-off frequency in contrast, and therefore the DV voltage and jitter of M are larger. Scheme A has lowest cut-off frequency without using equalizer.

5.7 Crosstalk effect for different schemes

For the three representative schemes, we also studied the crosstalk effect and Table 6 summarizes the eye openings and jitters with/without crosstalk. We see that generally, crosstalk noise does not hurt the eye quality. The eye opening of scheme B remains 0.14 V and jitter increases from 24.5 ps to 24.9 ps. Similarly, scheme M has the same eye opening and jitter with/without crosstalk. For scheme G, the jitter increases to 13 ps from 11 ps because the crosstalk affects the signal arrival time on the victim, and

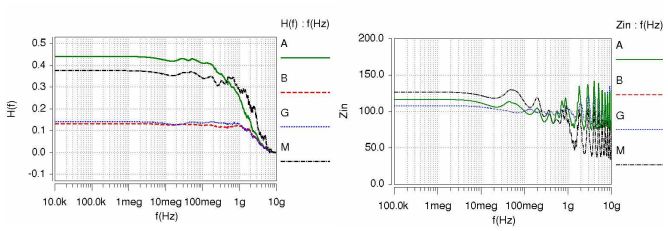

Figure 8. For channels with equalizer: (a) transfer function, (b) input impedance

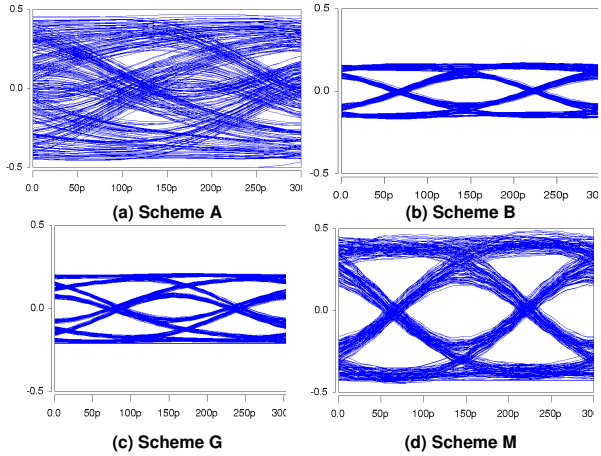

Figure 9. Eye diagram at output considering crosstalk

the eye opening reduces from 0.147 V to 0.143 V. The eye diagrams at the receiver input (output port) including the effect of the cross talk noise are depicted in Fig. 9.

6. Conclusion

Several types of low power passive equalizer is proposed and optimized in this work. The equalizer topologies include T-junction, parallel R-C and series R-L structures. These structures can be inserted at driver or/and receiver side at either the chip or package level and the communication bandwidth can be improved with little overhead on power consumption.

Using the area of the eye as the objective function to be maximized, we optimized these equalizers for the CPU-memory interconnection of an IBM POWER6^{TM} System with and without practical constraints on the RLCG parameter values. Our experimental

Table 6. Performance wi/wo crosstalk

Idx	without crosstalk		with crosstalk	
	V_{eye}	$Jitter$	V_{eye}	$Jitter$
B	0.140	24.5	0.140	24.9
G	0.147	11.1	0.143	13.0
M	0.307	26.8	0.307	26.8

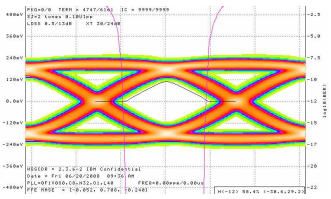

Figure 10. Eye diagram at output when using 3-tap FFE

results show that without employing any equalizers, the data-eye is closed for a bit-rate of 6.4Gbps. We tried twelve different equalizer schemes and found they produce very different eye diagrams. The scheme yielding the maximum eye improves the height of the eye to more than 300mV at a total power cost of 7.2mW, while the scheme yielding the minimum jitter limits the jitter magnitude to 10ps at a total power cost of 9.5mW. We also have shown that the solution resulting from the proposed optimization approach have very small sensitivity to the tolerance of the R,L,C values and the magnitude of the coupled noise.

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