

Bufferless Routing in Optical Gaussian Macrochip Interconnect

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Outline

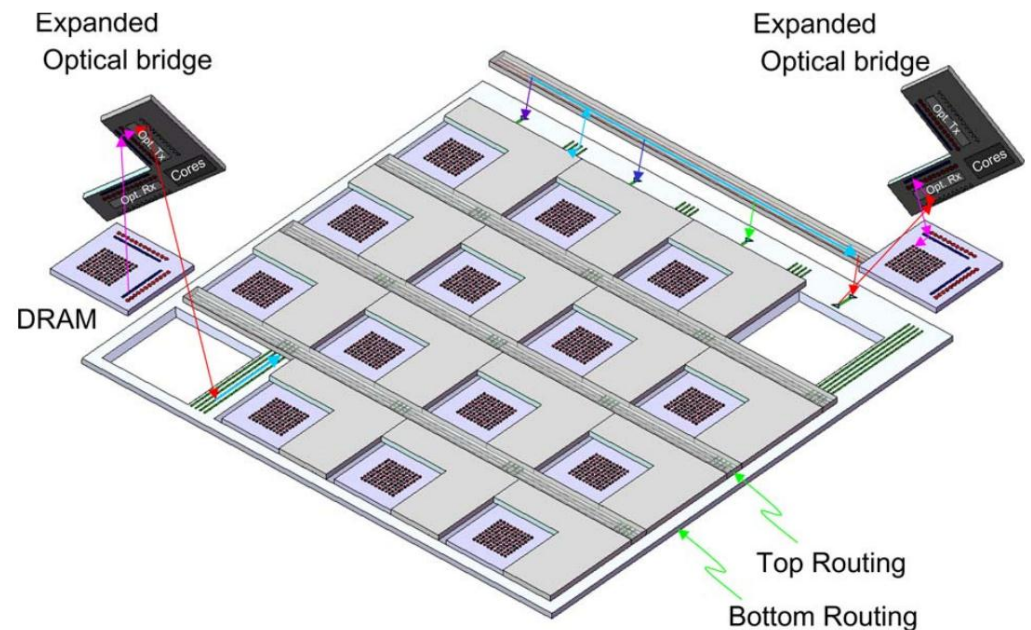
- Macrochip and bufferless routing in macrochip
- Gaussian network and Gaussian routing algorithm
- All-optical router design
- Performance evaluation
- Conclusion

Macrochip

- The macrochip is a large piece of silicon substrate where multiple chips are embedded and interconnected by a network.

Macrochip Features:

- Each site contains processor, DRAM chip and optical bridge chip
- Etched optical waveguides
- Fully connected network



Networks for Macrochip

- Problems with fully connected network.
- 1. Unacceptable wiring density, $N(N-1)$ separate channels.
- 2. Low port bandwidth.
- 3. Long transmission delay.
- Challenges of adopting low-radix network.
- 1. No optical random access buffer (RAM).
- 2. O/E/O conversion is extremely power-hungry.
- 3. Circuit switching network is of low network utilization.

Bufferless Routing in Macrochip

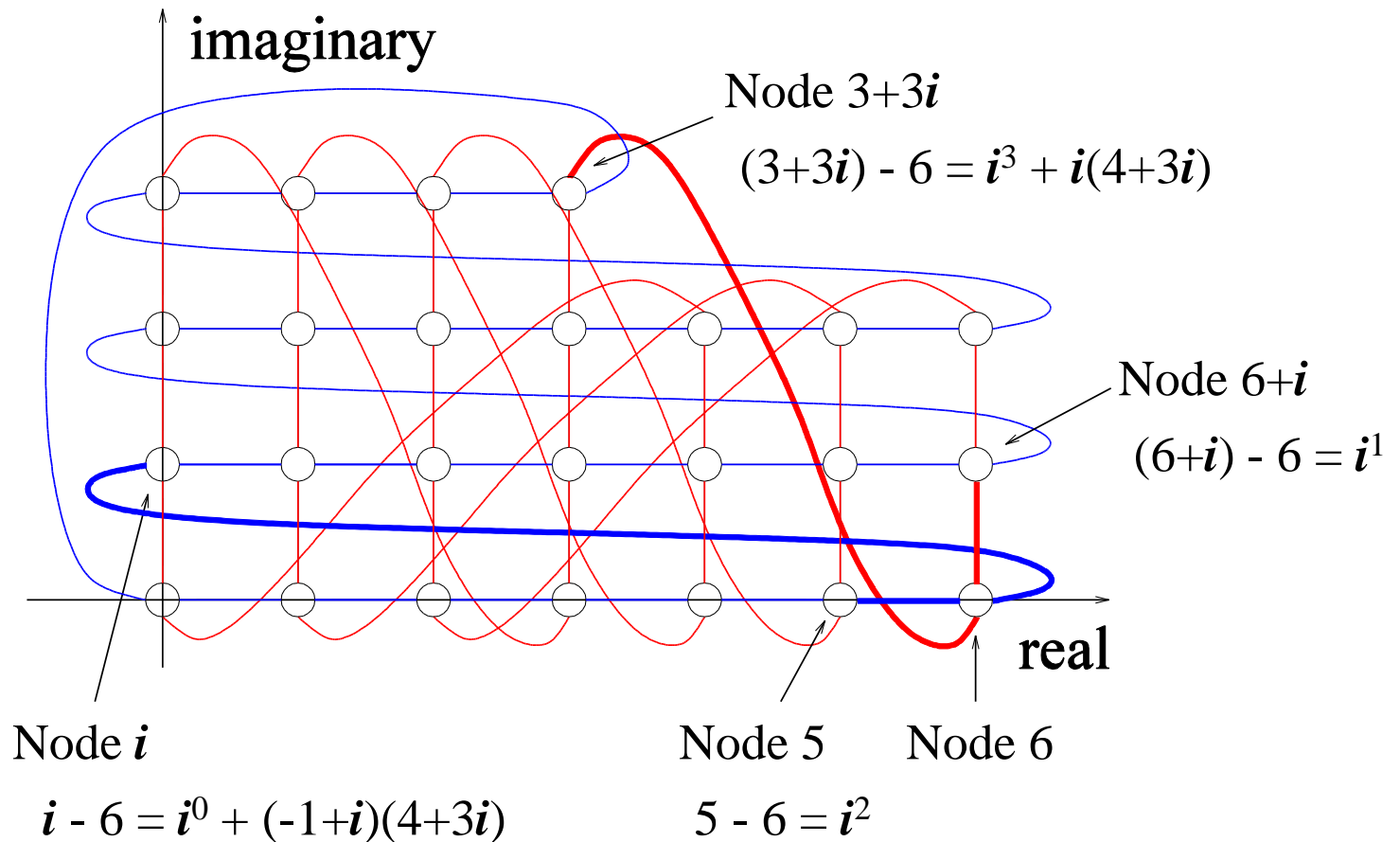
- Bufferless routing features.
- 1. Each incoming packet is assigned an output port.
- 2. Allow packets to be misrouted.
- 3. Avoidance of livelock.
- Requirements in macrochip.
- 1. Fast routing decision: hundreds of ps .
- 2. Small macrochip size.
- Execution time of Oldest First algorithm: $3 ns$.

Gaussian Network

- Gaussian network is a low-radix network defined in terms of Gaussian integer.
 - Related terminologies:
 - 1. Gaussian integer: Complex number with integral real and imaginary parts, for example, $4+3i$.
 - 2. A Gaussian network generated by $a+bi$ is denoted as G_{a+bi} .
 - G_{a+bi} interconnection:
 - A link exists between n_1 and n_2 if $n_1-n_2=i^j+(x+yi)(a+bi)$, $j=0, 1, 2$ and 3 .

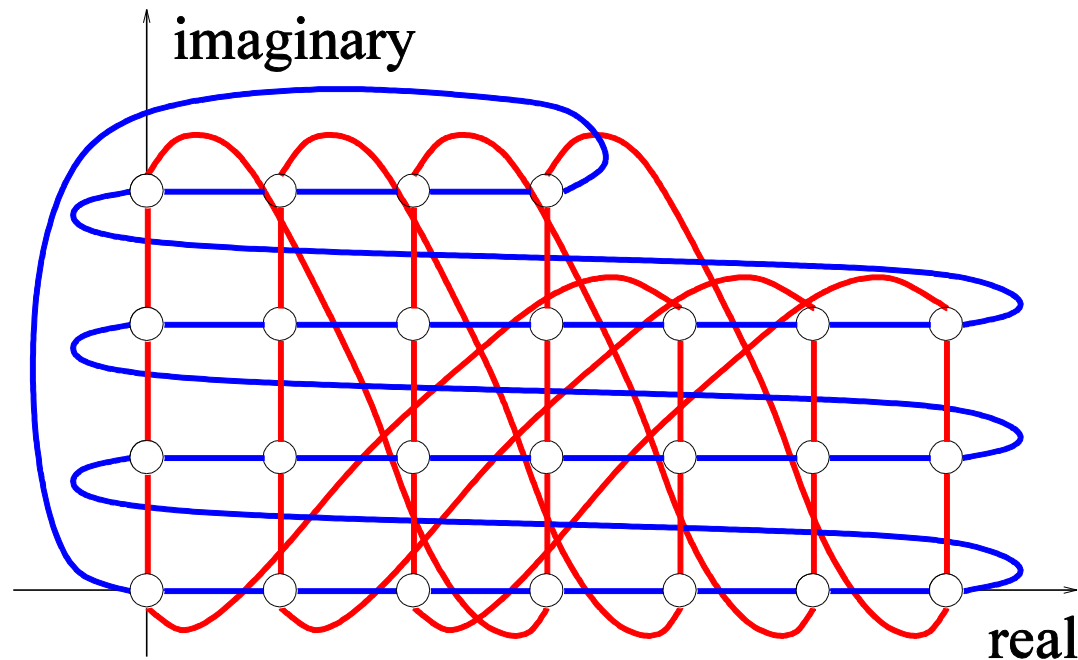
An Example of G_{4+3i}

- Nodes 6 and i are neighbors as $i - 6 = i^0 + (-1+i)(4+3i)$.



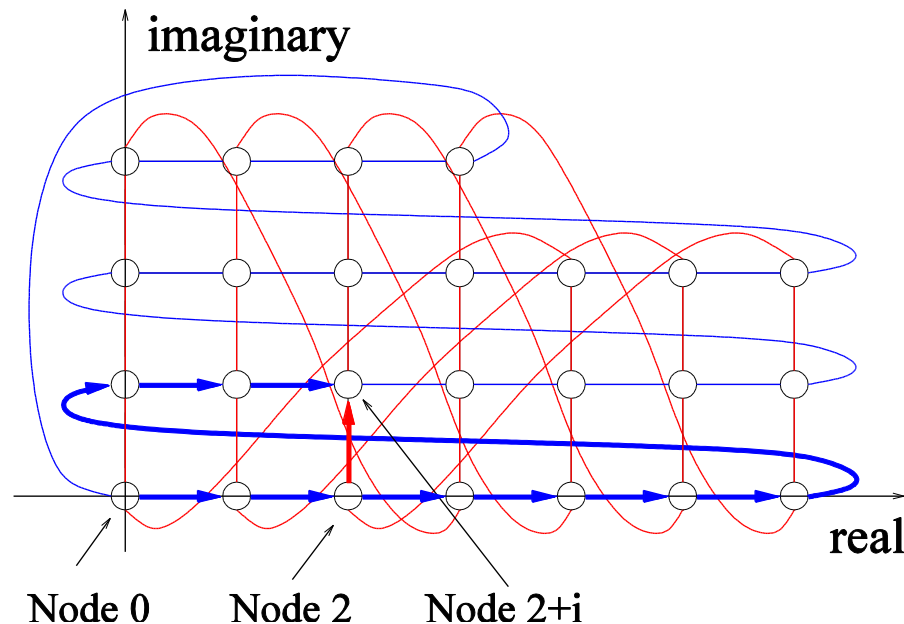
Hamiltonian Cycles in G_{a+bi}

- When a and b are coprime, G_{a+bi} can be decomposed into two edge-disjoint Hamiltonian cycles.
- Two Hamiltonian cycles in G_{4+3i} .



Gaussian Routing Algorithm

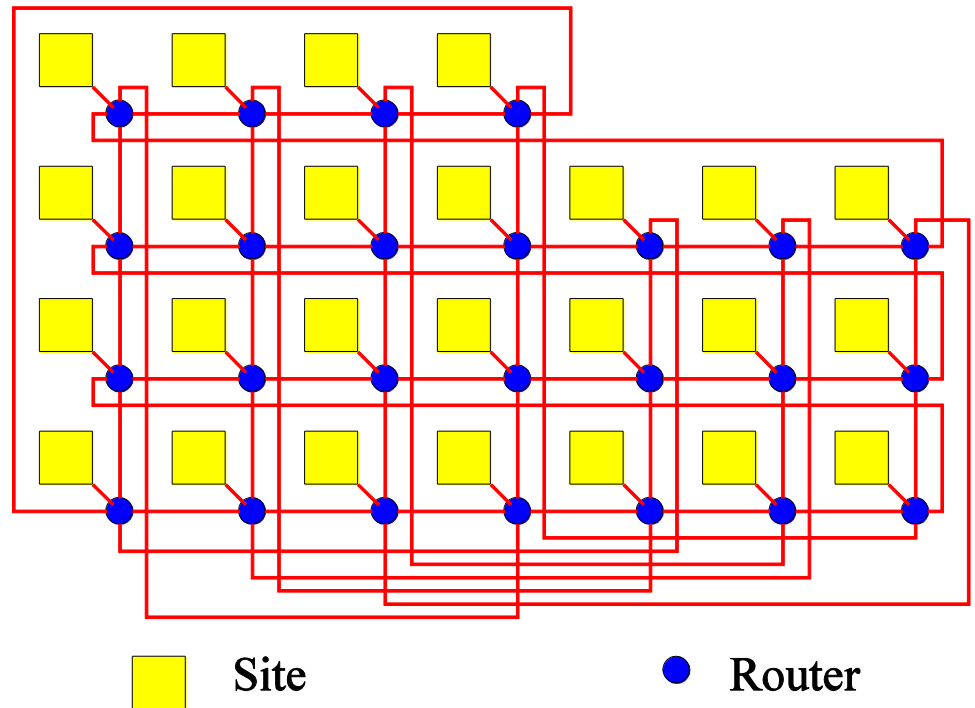
- No output port contention if packets are routed along Hamiltonian cycles.
- Gaussian routing algorithm:
 1. Shortest routing path in the absence of output port contention.
 2. Packets failing output port contention are routed along one Hamiltonian cycle.
- Example of Gaussian routing from 0 to $2+i$ in G_{4+3i} .



Gaussian Macrochip

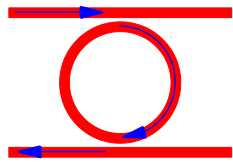
- In Gaussian macrochip, each site is attached to a router. All routers are interconnected by a Gaussian network.

- An example of Gaussian macrochip adopting G_{4+3i}



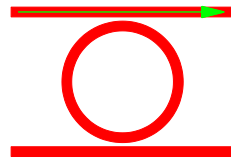
All-Optical Router Design

Two states of microring resonator



$$\lambda_s = \lambda_r$$

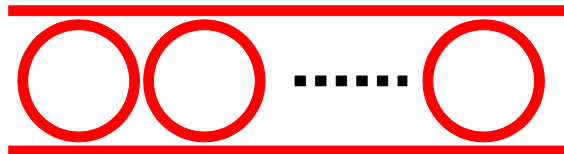
ON state



$$\lambda_s \neq \lambda_r$$

OFF state

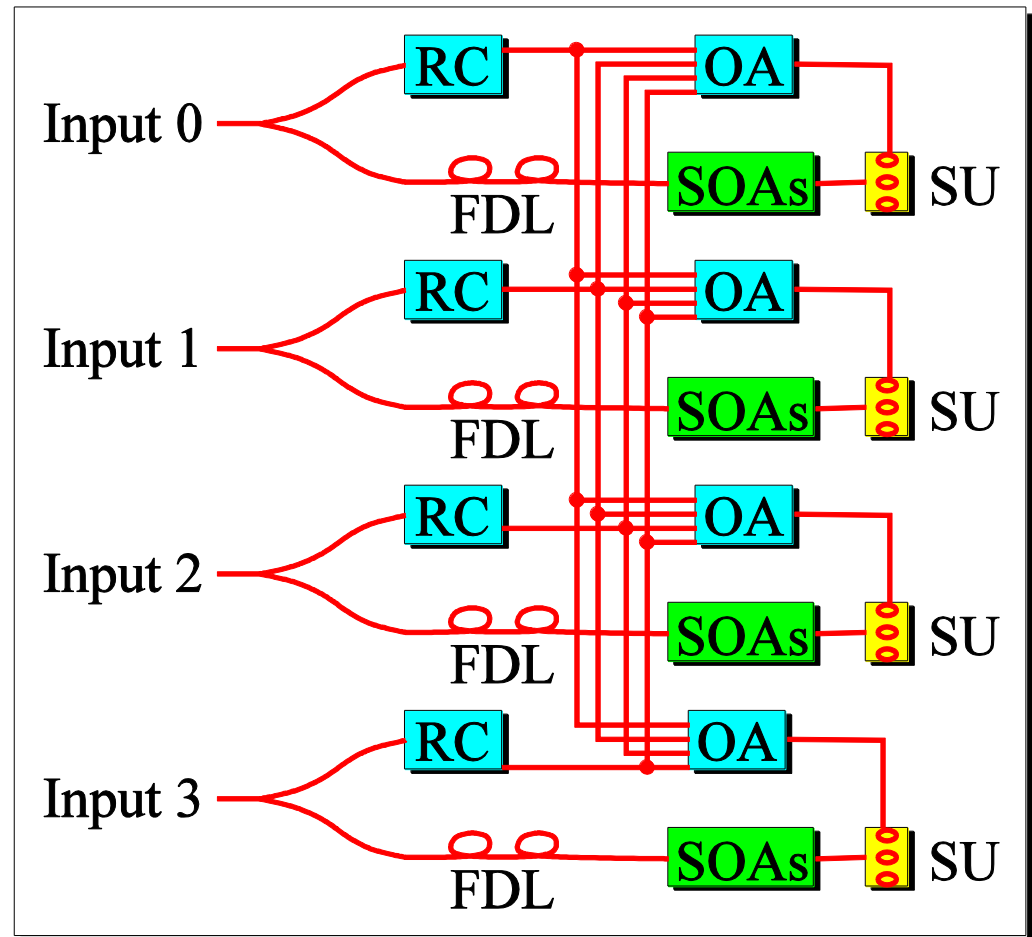
WDM switch with multiple microring resonators



- Features:
- 1. Compact size (a few μm)
- 2. Fast switching time ($30 ps$)
- 3. Low power consumption ($0.5 mW$)

All-Optical Router Architecture

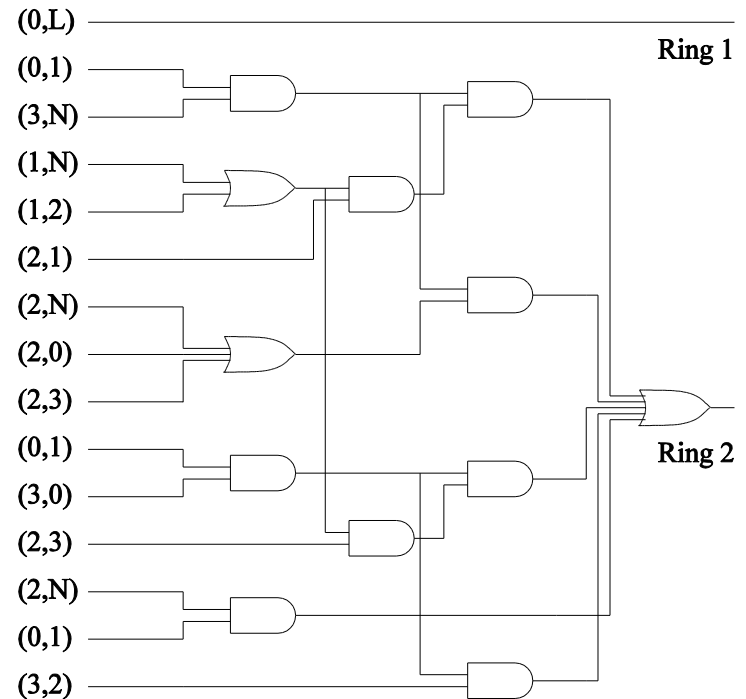
- RC: routing computation
- OA: output allocator
- SU: switching unit
- FDL: fiber delay line



Hardware Implementation

- Logic circuit controlling switching unit.

Ring	0 ROP	1 ROP	2 ROP	3 ROP
1	L	X	X	X
2	1	X	$N/0/3$	N
	1	$N/2$	1	N
	1	X	N	0
	1	$N/2$	3	0
	1	X	X	2
3	3	N	$N/0/1$	X
	3	N	3	$N/2$
	3	0	N	X
	3	0	1	$N/2$
	3	2	X	X



Power Consumption Analysis

- Switching unit power consumption: 0.5 W
- SOA power consumption: 65 mW.

OPTICAL LOSS PARAMETERS FOR MACROCHIP

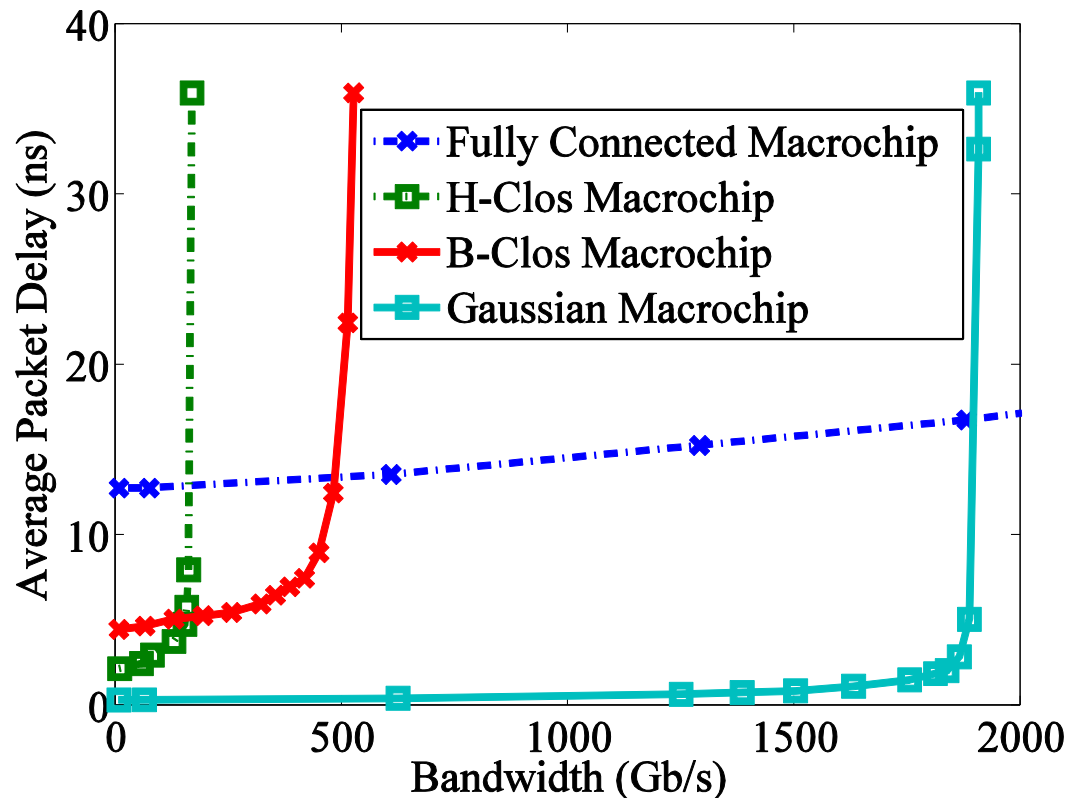
Photonic Device	Optical Loss (dB)
Modulator Insertion	4
Waveguide (per <i>cm</i>)	0.05
Pass by ring	0.005
Drop into ring	1.5
Coupler	1
Splitter	0.2

Performance Evaluation

- Four types of macrochips:
 - 1. Fully connected macrochip
 - 2. H-Clos macrochip
 - 3. B-Clos macrochip
 - 4. Gaussian macrochip
- Simulation configuration:
 - 1. 64 parallel optical waveguides
 - 2. 64 wavelengths per optical waveguide
 - 3. Off-chip laser power: 33 W
 - 4. Thermal tuning power per microring resonator: 0.01 mW

Average Packet Delay Performance

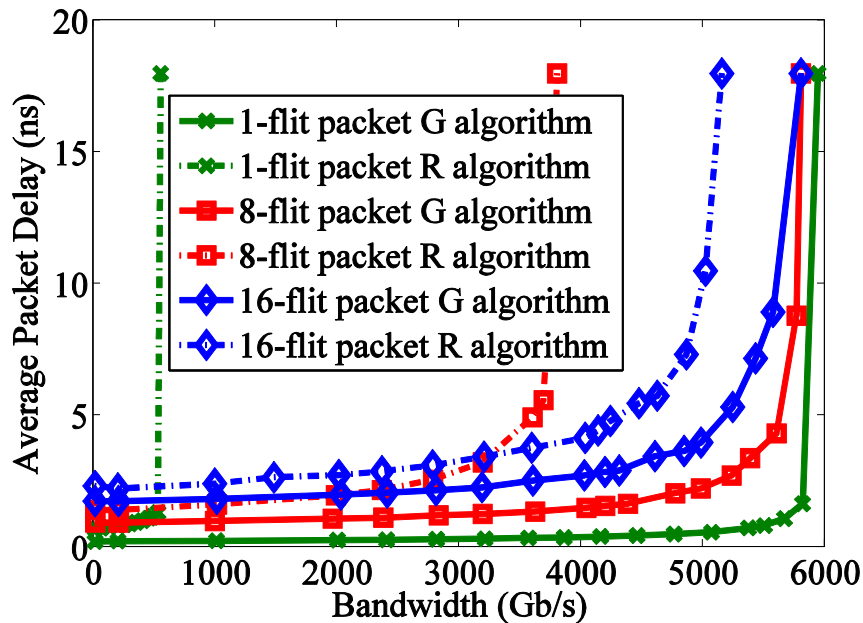
- Comparison among four types of macrochips.
- 1. Gaussian macrochip has much higher port bandwidth under equal wiring density.
- 2. The transmission delay is much lower for Gaussian macrochip.



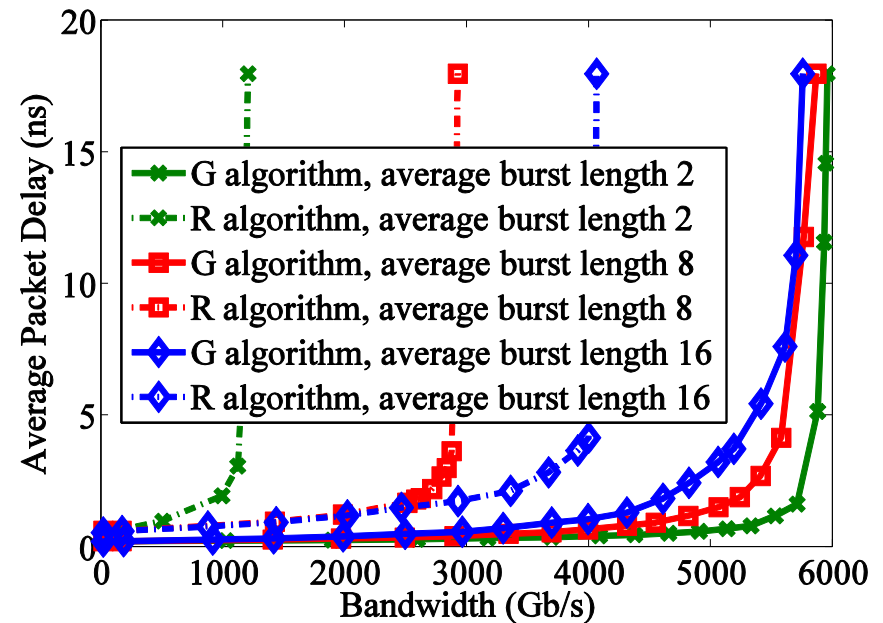
Reserve Routing Algorithm

- 1. Reserve routing algorithm has poor performance when packet size is small or burst length is short.
- 2. Large-size packet or long burst is needed to compensate for the path establishment overhead.

Uniform random traffic in G_{4+3i} with 25 nodes

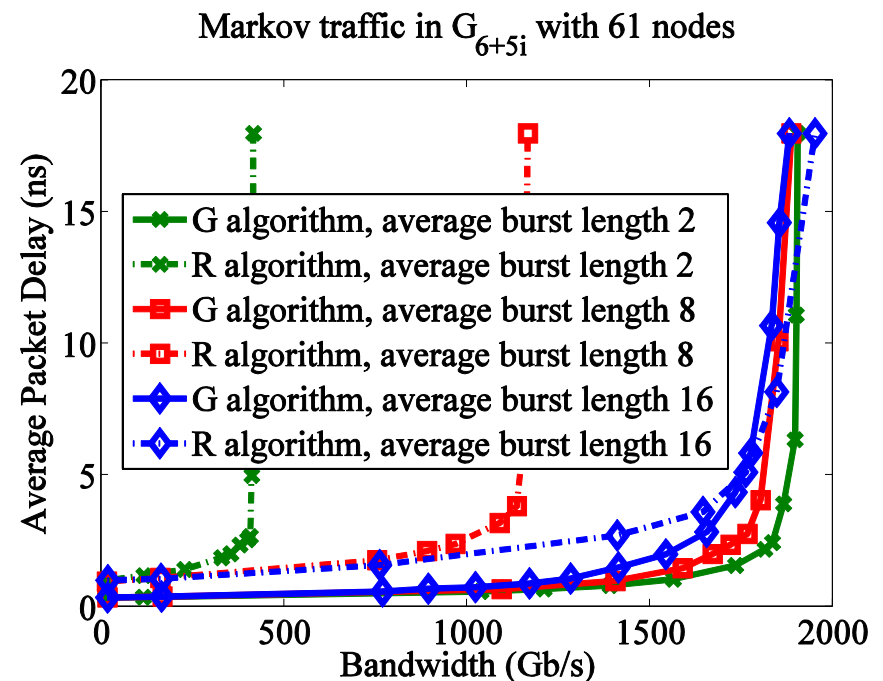
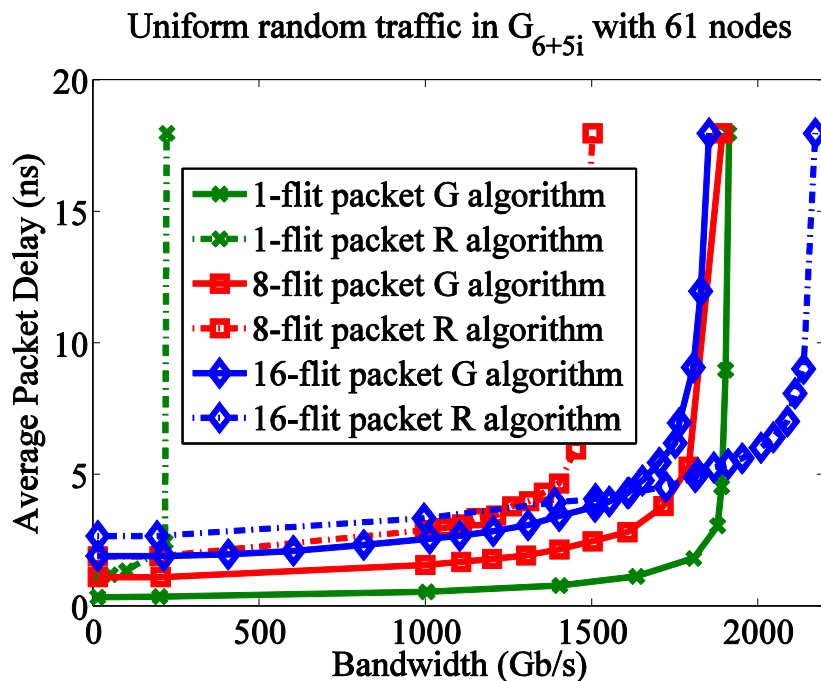


Markov traffic in G_{4+3i} with 25 nodes



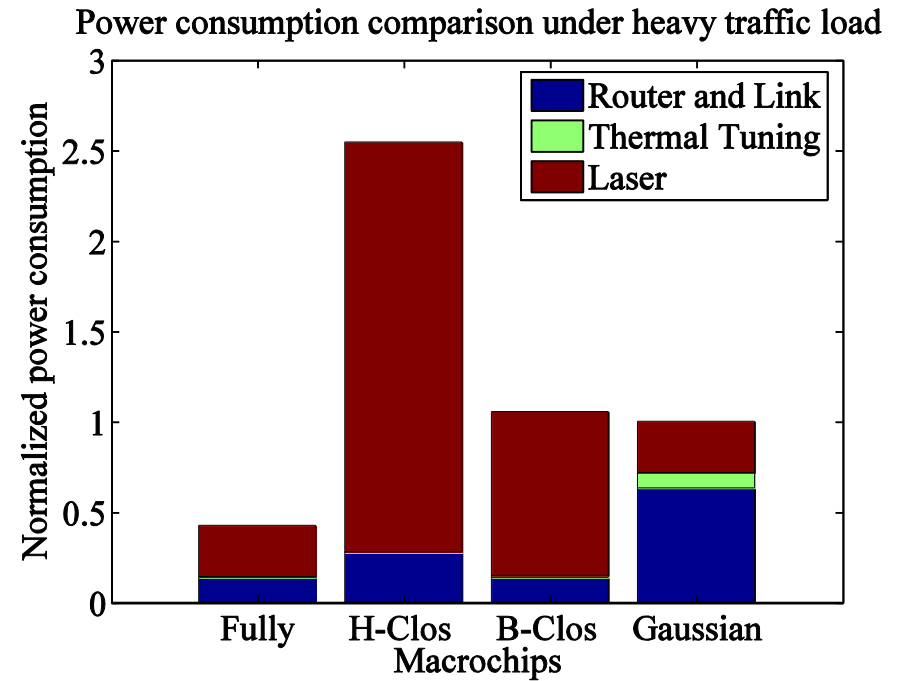
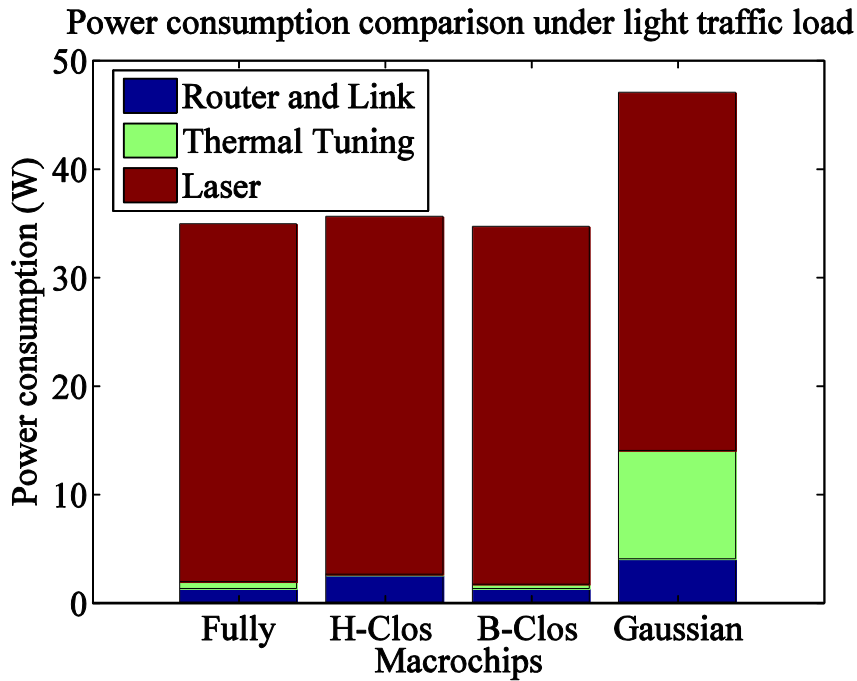
Reserve Routing Algorithm

- Simulation results are similar in Gaussian macrochip with 61 sites.



Power Consumption Performance

- Gaussian macrochip is more power efficient than B-Clos and H-Clos macrochips under heavy traffic load.



Conclusion

- We propose Gaussian macrochip, which adopts low-radix Gaussian network.
- We propose Gaussian routing algorithm to overcome the lack of optical RAM.
- An all-optical router is designed to implement Gaussian routing algorithm in hardware.
- Gaussian macrochip supports higher communication bandwidth and achieves lower communication delay.
- Gaussian macrochip is more power-efficient than H-Clos and B-Clos macrochips under heavy traffic load.

Thank You!

Acknowledgement

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Website: <http://mcl.cewit.stonybrook.edu/>