Enhanced Overloaded CDMA Interconnect (OCI) Bus Architecture for on-Chip Communication

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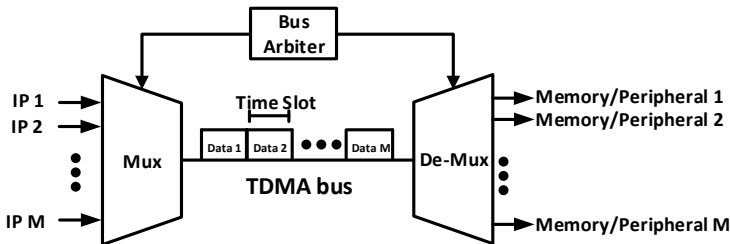Alexandria University

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Outline

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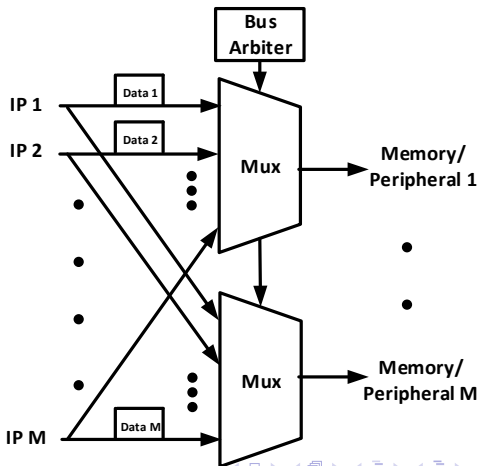
Time Division Multiple Access (TDMA)

- In TDMA: Bus access is time shared.
- Arbitration overhead increases with the number of cores.
- Capacity is limited by the number of time slots.

Space Division Multiple Access (SDMA)

- In SDMA: point to point connection by crossbars.
- Best connectivity at the expense of quadratic complexity.
- Capacity is limited by the complexity.

Outline

Code Division Multiple Access (CDMA)

- In CDMA: Bus access is code shared.
- Each core has a unique N chip spreading code
- The data from each core is spread by XORing the data with each chip in the spreading code.
- The spreading codes are summed and sent serially on the bus.
- Data can be extracted from the bus by correlating with the signature code.
- CDMA requires a single user receiver (Matched filter).
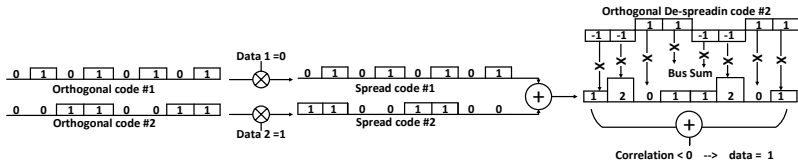
Conventional CDMA bus

- Data is XORed with the spreading code.
- All spreading codes are summed.
- Correlation is done using two accumulators.
- The accumulator with the larger value determines the sent bit.
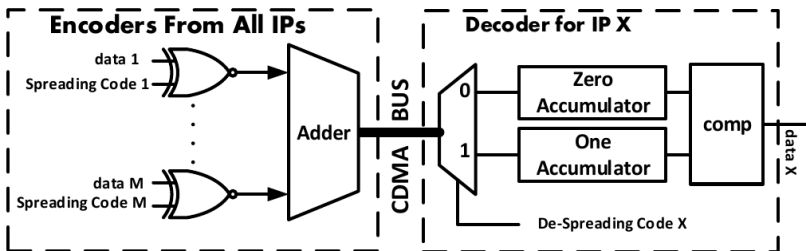
## Why CDMA for On-Chip Interconnects ?

- CMDA for on-chip interconnects is not fully explored yet, leaving a room for optimization
- As shown in this paper, the bus capacity and bandwidth can be easily increased by applying some new innovative ideas.
- In this work, we aim to increase the capacity without increasing the complexity.

Outline

Non-Orthogonal Pair Difference (PD) codes

- In the orthogonal code set, The difference between two consecutive bus sums is always even, we call it the pair difference (PD).
- Non-orthogonal codes can be added on the bus that alters the modulo 2 of PD.
- The modulo 2 of PD can thus determine the data encoded in the non-orthogonal code.
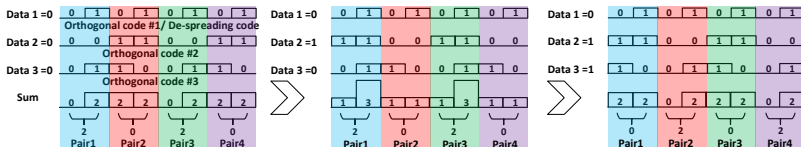
- For a spreading code set of length N chips, there are only $N/2$ pairs of chips.
- Therefore, there can exist only $N/2$ PD codes.
- The codes can be generated by the formula $PD[l] = 2^{7-2l}$, $0 \le l < N/2$.

$$PD[0] = 2^7 = \{1, 0, 0, 0, 0, 0, 0, 0\}$$
$$PD[1] = 2^5 = \{0, 0, 1, 0, 0, 0, 0, 0\}$$
$$PD[2] = 2^3 = \{0, 0, 0, 0, 1, 0, 0, 0\}$$
$$PD[3] = 2^1 = \{0, 0, 0, 0, 0, 0, 1, 0\}$$

Outline

Overloaded CDMA Bus

Implementation

- We propose an overloaded CDMA architecture based on the PD codes, thus called the Difference-OCI (D-OCI)
- Full capacity bus implemented on AC701 FPGA kit.
- Two architectures are implemented: reference and pipelined architectures.

Hybrid Encoder
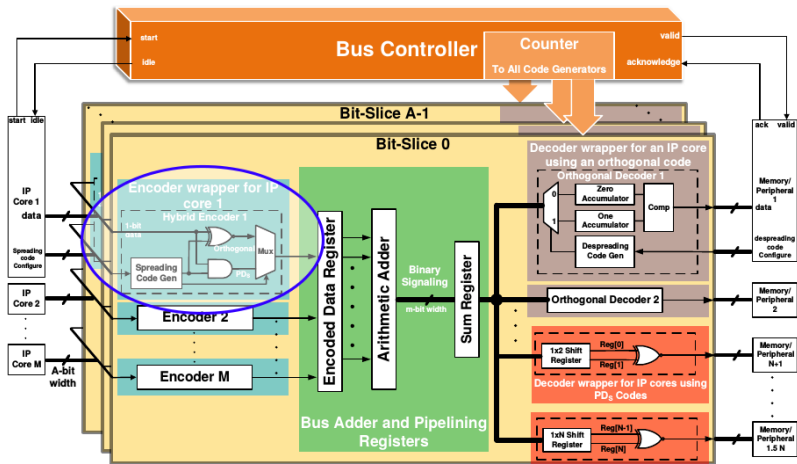
Hybrid Encoder

- The encoder is AND gate.
- If data is 0 send a stream of 0, the pair difference remains even.
- If data is 1 send a non-orthogonal PD code causes the pair difference to be odd.
- The modulo 2 of the pair difference is detectable.

Binary Bus Adder
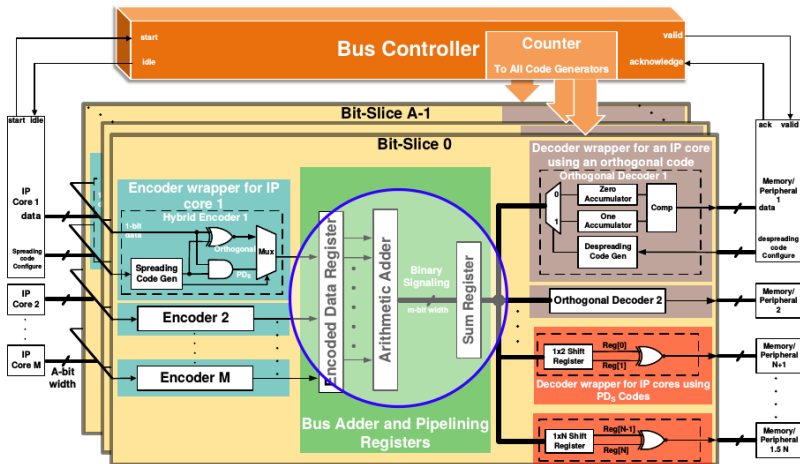
Binary Bus Adder

- Adds the encoded chips from all encoders.
- The sum produced by the adder is passed to all decoders.
- Surrounded by two pipeline register isolating the critical path in the adder.

Decoders
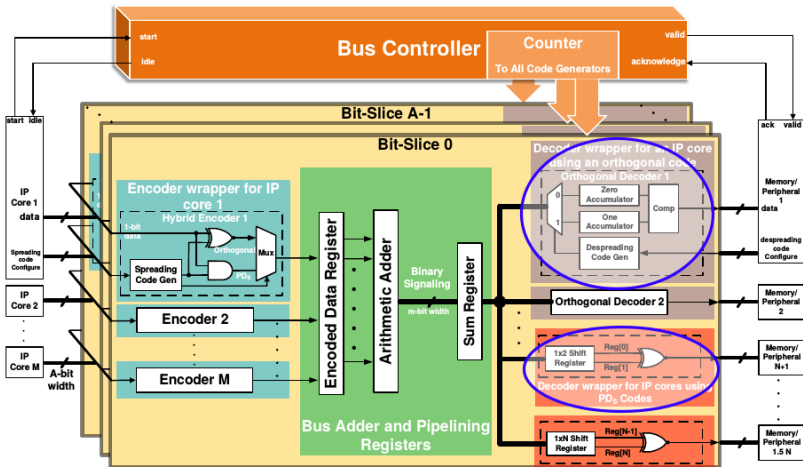
Decoders

- The orthogonal code decoders resemble the decoder employed in conventional CDMA.
- The PD code decoders employ an XOR gate to determine the modulo 2 of the pair difference.
- The inputs to the XOR gate are the LSBs of the bus sums in a pair.
- A register is used to hold the incoming LSBs of the bus sum.

Outline

1. **Background**
   - From T/SDMA to CDMA
   - Conventional On-Chip CDMA Bus

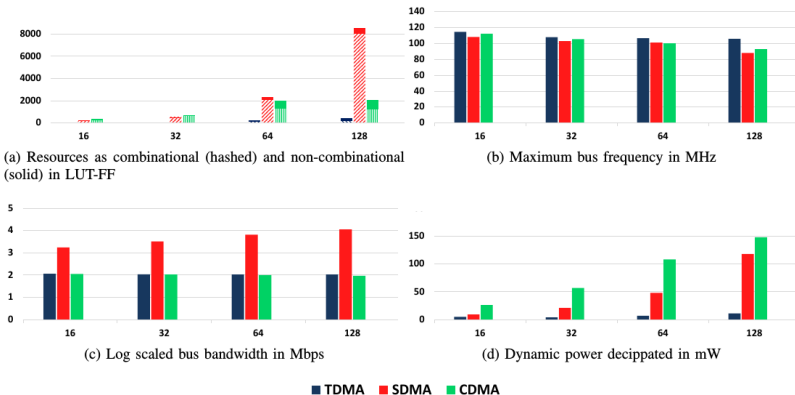2. **Overloaded CDMA Interconnect (OCI)**
   - Pair difference codes
   - Proposed Bus Architecture

3. **Results**
   - T/SDMA vs CMDA
   - Performance

4. **OCI vs AXI**
   - High Level Synthesis (HLS) OCI Bus
   - D-OCI vs AXI results

5. **Conclusions and Future Work**

T/SDMA vs CMDA

(a) Resources as combinational (hashed) and non-combinational (solid) in LUT-FF

(b) Maximum bus frequency in MHz

(c) Log scaled bus bandwidth in Mbps

(d) Dynamic power decippated in mW

■ TDMA   ■ SDMA   ■ CDMA

T/SDMA vs CMDA

- Conventional CDMA utilizes a higher area than TDMA but offers equivalent bandwidth.
- Conventional CDMA provides lower bandwidth than SDMA but consumes much smaller area.
- OCI bus can improve the bandwidth and reduce the area per IP core.
- We compare the conventional CDMA to T/SDMA, we then compare the D-OCI the conventional CDMA along with the M-OCI developed in our previous work.

Outline

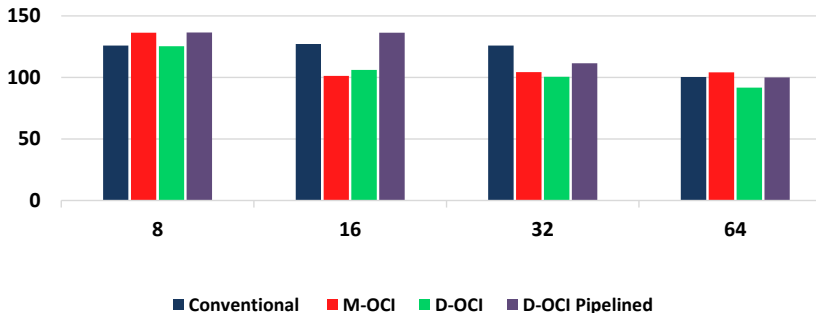## Area

- Number of IPs is 50% more.
- The extra area is small compared to extra IPs.
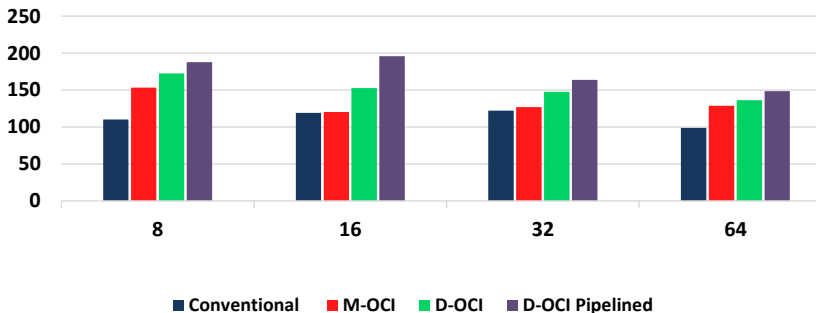- Area per IP is reduced.

■ Conventional ■ M-OCI ■ D-OCI ■ D-OCI Pipelined
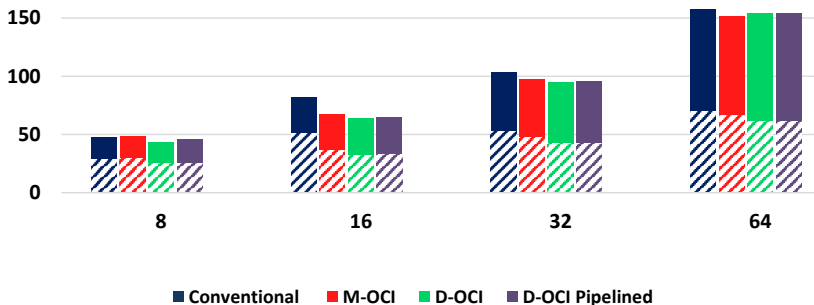
Frequency

- Computation path is increased.
- The maximum frequency decreased.
- Can be fixed by pipelining the bus adder.

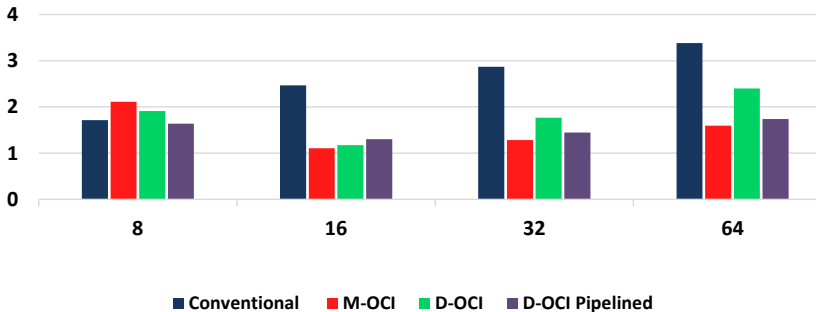■ Conventional ■ M-OCI ■ D-OCI ■ D-OCI Pipelined

Bandwidth

- The number of sent bits increased by %50.
- Bandwidth increased.

Power Consumption

- Area per IP is reduced.
- So power per IP is reduced.

■ Conventional   ■ M-OCI   ■ D-OCI   ■ D-OCI Pipelined

Outline

HLS OCI Bus

- The AXI bus is widely deployment in modern SoCs, it is extensively supported by different vendors and CAD tools and supports both TDMA and SDMA bus access.
- To compare the OCI to the AXI, we implemented a D-OCI HLS IP using the Vivado HLS tool.
- OCI and AXI implemented and validated on the Zedboard Zynq-7000 SoC

OCI vs AXI testbed

Outline

D-OCI vs AXI results

Bus Topology	Bus Capacity $M \times M$	LUTs	FFs	Latency clock cycles	Frequency MHz	Bandwidth Gbps
D-OCI N = 8	11×11	177	222	13	109	2.951
D-OCI N = 16	23×23	487	567	22	113	3.78
AXI SAMD-Crossbar	11×11	8,229	5,651	42	104	0.871
AXI SAMD-Crossbar	16×16	11,299	7,833	61	93	0.78
AXI SASD-TDMA	11×11	2,123	1,761	122	107	0.309
AXI SASD-TDMA	16×16	2,919	2,532	177	105	0.304

D-OCI vs AXI results

- The D-OCI bus contains only the write channel while the AXI contains read, write and write response channels.
- This causes the magnitude difference in utilization of the D-OCI bus over AXI Shared Address Shared Data (SASD) bus.
- D-OCI demonstrates the lowest latency since addressing the slaves is done once before the data transaction.
- AXI Shared Address Multiple Data (SAMD) demonstrates higher transaction latency than the D-OCI since the addressing is done in sequence.
- AXI SAMD should demonstrate lower latency than the D-OCI in burst access mode.

Conclusions

- On-Chip CDMA is not fully explored yet.
- CMDA capacity can be boosted by 50% using orthogonal signature code properties.
- The OCI can be used as the core interconnect of buses and NoCs.

Future Work

- Architectural enhancements: pipelining, resource sharing.
- Explore more signature code properties.

Thank You